



# JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh, India

R-13 Syllabus for ECEJNTUK

III Year-I Semester	DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS(RT31044)	T	P	C
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## Prerequisite Course:

STLD

## Course Description and Objectives:

The student will be introduced to

- The electrical behavior of CMOS both in static and dynamic conditions and before that study the diode/transistor-transistor logic and Emitter coupled logic.
- In this course, students can study Integrated circuits for all digital operational designs like adder, subtractor, multipliers, multiplexers, registers, counters, flip flops, encoders, decoders and memory elements like RAM and ROM.
- Design and to develop the internal circuits for different digital operations and simulate them using hardware languages using integrated circuits.
- Understand the concepts of SSI Latches and Flip-Flops and Design of Counters using Digital ICs, modeling of sequential logic integrated circuits using VHDL.

## Course Outcomes:

Upon completion of the course, the student will be able to achieve the following outcomes.

Cos	Course Outcomes	POs
1	Understand the concepts of different logics and implementations using Integrated circuits..	3
2	Design and analyze any Digital design in real time applications signal generating circuits.	3
3	Extend the digital operations to any width by connecting the ICs and can also design, simulate their results using hardware description language.	3
4	Understand the concepts of MSI Registers and Modes of Operation of Shift Registers, Universal Shift Registers.	3

## Syllabus:

### **Unit-I:**

**Digital Design Using HDL:** Design flow, program structure, History of VHDL, VHDL requirements, Levels of Abstraction, Elements of VHDL, Concurrent and Sequential Statements, Packages, Libraries and Bindings, Objects and Classes, Subprograms, Comparison of VHDL and Verilog HDL.

### **Unit-II:**

**VHDL Modelling :** Simulation, Logic Synthesis, Inside a logic Synthesizer, Constraints, Technology Libraries, VHDL and Logic Synthesis, Functional Gate-Level verification, Place and Route, Post Layout Timing Simulation, Static Timing, Major Netlist formats for design representation, VHDL Synthesis-Programming Approach.

### **Unit-III:**

**Programmable Logic Devices (PLDs) & Memories:** Programmable Read Only Memory, Programmable Logic Array, Programmable Array Logic Devices, ROM: Internal structure, 2D-Decoding, Commercial ROM types, timing and applications,. Static RAM: Internal structure, SRAM timing, standard, synchronous SRAMS, Dynamic RAM: Internal structure, timing, synchronous DRAMs. Design considerations of PLDs with relevant Digital ICs.

**Unit-IV:**

**Digital Logic Families and Interfacing:** Introduction to logic families, CMOS logic, CMOS steady state and dynamic electrical behavior, CMOS logic families, bipolar logic, transistor-transistor logic, TTL families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing, Emitter coupled logic.

**Unit-V:**

**Combinational Logic Design:** Adders & Subtractors, Ripple Adder, Look Ahead Carry Generator, Binary Parallel Adder, Binary Adder-Subtractor, ALU, Decoders, encoders, three state devices, multiplexers and demultiplexers, Code Converters, parity circuits, comparators, multipliers, Barrel Shifter, Simple Floating-Point Encoder, Cascading Comparators, Dual Priority Encoder, Design considerations with relevant Digital ICs, modeling of Circuits by using VHDL.

**Unit-VI:**

**Sequential Logic Design:** SSI Latches and Flip-Flops, Counters, Design of Counters using Digital ICs, Ring Counter, Johnson Counter, Modulus N Synchronous Counters, MSI Registers, Shift Registers, Modes of Operation of Shift Registers, Universal Shift Registers, MSI Shift Registers, Design considerations with relevant Digital ICs, modeling of circuits by using VHDL.

**TEXT BOOKS:**

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 3rd Edition, 2005.
2. Designing with TTL Integrated Circuits: Robert L. / John R. Morris & Miller.

**REFERENCES:**

1. "Fundamentals of Digital logic design with VHDL". Stephen Brown & Zvonko Vranesic, Tata McGraw Hill, 2<sup>nd</sup> edition.

**VHDL Primer – J. Bhasker, Pearson Education/ PHI, 3rd Edition**